Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**GATE**

**.085”**

**.104”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: G = .020” X .025”**

**Backside Potential: Drain**

**APPROVED BY: DK DIE SIZE .085” X .104” DATE: 5/3/22**

**MFG: INFINEON THICKNESS .014” P/N: IRFC9034NB**

**DG 10.1.2**

#### Rev B, 7/19/02